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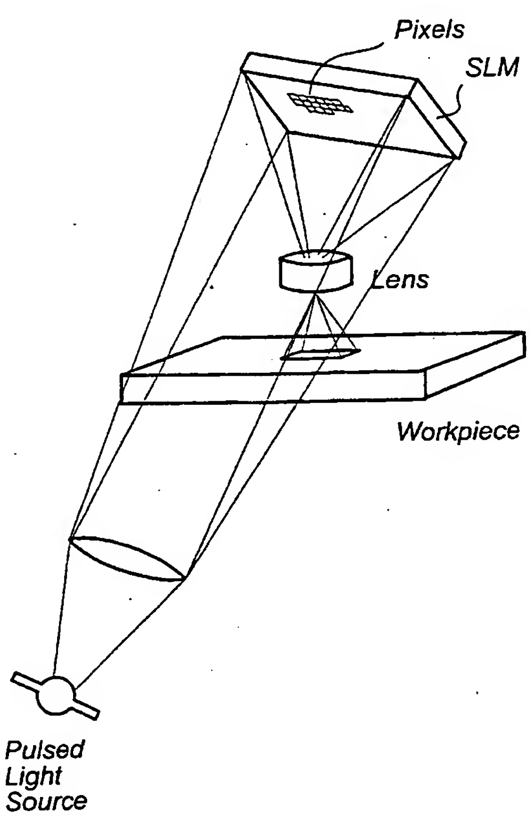

(57) Abstract: A high-speed datapath for a high-performance pattern generator such as an analog SLM for generating the image is disclosed. The data path has provisions for completely independent parallel data flows giving true scalability to arbitrarily high throughput. In a preferred embodiment areas on the SLM are assigned to specific rasterizing and fracturing processors. There is an overlap between fields for blending of the edges in the pattern and for computation of interaction between features in the pattern. The datapath has data integrity checks and a recovery mode when an error condition is raised, allowing it to recover from most errors without creating new errors.

WO 01/18606 A1

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DATA PATH FOR HIGH PERFORMANCE PATTERN GENERATOR

Field of the invention

The present invention relates to high-end pattern generation, such as for the patterning of photomasks, microelectronic and microoptical devices and for production of display devices. Other applications of highly precise patterns such as security printing and interconnection devices are also related to the invention.

The term pattern generator is used in the description to mean a machine that creates a physical pattern from data, typically by the action of light on a photosensitive surface.

Background

Patterning of photomasks for the production of integrated circuits is developing according to the so-called More's law, where every three years a new circuit generation with four times the complexity of the previous one is created. Thirty-five years ago the patterns were manually cut with knife in a red plastic film, so called Rubylith film. Later the need for increasingly precise and complex patterns led to the development of the optical pattern generator with a computer-controlled stage and flash lamp that exposed a series of rectangles on emulsion film. In the mid eighties the e-beam and optical raster-scanning pattern generators were invented and have since provided masks with astounding accuracy and feature density. However, being in principal serial devices, the raster scanning pattern generators are approaching their end of economical life. What is needed is a radically new writing principle that can keep up with the exponential growth of complexity predicted by More's law.

In a series of pending PCT patent applications (SE99/00310 and others) one of the inventors (Sandström) has disclosed a novel type of pattern generator with advantages in resolution, precision and throughput over any other previously known systems. The present invention is a data path with extremely high data capacity to be used in said new type of pattern generator. Another aspect of the invention is the provisions for calibrations and real-time data corrections that make the new pattern generator highly precise even at very high speeds.

Object of the invention

It is therefore an object of the present invention to provide a method and an apparatus to alleviate the above-discussed problems with the prior art.

This object is achieved by means of a method and an apparatus according to the enclosed claims.

Brief description of the drawings

Fig 1 shows prior art: (a) a pattern generator using a scanning laser and (b) a multiprocessor-multibeam where each processor sends data to each one of the beam interfaces.

Fig 2 shows a generic pattern generator using an spatial light modulator for creating the image.

Fig 3 shows a multiprocessor architecture with multiple fracturing processors and multiple rasterization processors each creates data for a contiguous area in the SLM.

Fig 4 shows a completely parallel architecture with two completely independent units each with several fracturing processors and several rasterizing processors feeding separate areas of the SLM.

Fig 5 shows how the input pattern is fractured with overlap accommodating both a physical overlap between

exposure fields and an interaction overlap for image processing, e.g. inverse convolution.

Fig 6 shows a preferred embodiment for loading the grey-scale bitmap into the SLM.

Fig 7 shows a preferred embodiment for pixel-by-pixel lookup for overlap generation and error correction.

Function of the invention In previously known pattern generators, as illustrated in fig 1a, a single beam writes the pattern and the capacity is limited by the amount of data that can be pushed through a single beam blanker or modulator. Schemes with multiple beams scanning in parallel are used to alleviate the limit on throughput. However, in a multibeam raster-scanning pattern generator, as illustrated in fig 1b, the pattern is interlaced between the beams, i.e. all beams write every part of the pattern. It is previously known to rasterize the beam data in a multiprocessor architecture, and typically each processor rasterizes a contiguous area of the pattern. The finished data must be divided according to the interlace structure of the beams and every processor must send pattern data to each beam. This adds considerable complexity and is a hurdle to true parallel processing of data. To achieve high throughput a system with several parallel busses or a cross-switch structure of parallel links are used. The approach is scalable only up to a limit where the principle of every processor sending data to every beam simply leads to too much crosswise data transfers. Adding more processors is always possible, but it is not always possible to increase the data flow in an architecture with much interdependence between different modules. One practical limit is when the rasterizer does not fit into a single backplane. Multiple synchronized backplanes with several parallel busses might be possible to build, but drives up overhead and ultimately the system cost.

We disclose a different rasterizer and an architecture which gives true scalability and allows every interface to be parallel. Data is split and sent to different processors and travel completely separate paths. The degree of necessary synchronisation is low and complete self-contained processing units can be added to increase the processing power.

Another aspect of the invention is that the highly parallel data channel has provisions for pattern correction of several types. Such correction increases the workload in all steps of the data processing and also increase the data flow considerably. In a typical raster-scan architecture this would be difficult to accommodate due to data transfer limitations and a lack of true scalability. With the truly scalable architecture disclosed here the cost of the data path grows linearly with the amount of work that needs to be done, but without other hard limits.

The invention is related to a pattern generator comprising a spatial energy beam modulator (SEBM) using any kind of energy beam, such as light, electron-beams etc. In the preferred embodiment described in the following, the invention is described as using a spatial light modulator (SLM). However, it would be appreciated by those versed in the art that several other alternative modulators are possible to use within the scope of the invention. Other modulators using a modulating area which changes in an analog mode to modulate the energy beam are parallel near-field lithography, which relates to direct exposure of resist with current, and modulators for massive parallel writing with electron-beams or ion-beams, either by using a modulator with an array of modulating elements together with a scanning system or by using large arrays of separate beams. Likewise it is known that massively parallel lithography can be performed with spatial modulation of soft x-ray or

extreme ultraviolet light using arrays of micro-mechanical shutters and diffractive lenses.

Preferred embodiments

Embodiments of the invention will in the following be described by way of examples. However, it should be appreciated by those versed in the art that the invention is not limited to these examples.

A preferred embodiment of the invention is a rasterizer for a high-end pattern generator (PG) for writing photomasks for the 0.13 μm "design node". The PG is capable of writing features down to 180 nm. The pattern generator is described in the PCT patent application SE99/00310 using an analog reflective micromechanical SLM and projecting the image of the SLM through a demagnifying lens onto the mask blank, as is illustrated schematically in Fig 2. The SLM has the array size 2048 x 512 pixels and each pixel is 16 x 16 μm wide. The lens has the demagnification 160X and the projected size of an SLM pixel is 0.1 x 0.1 μm. The analog pixels of the SLM are driven by a voltage with more than 50 levels, and preferably 65 levels, between full and zero exposure, corresponding to an address grid of 0.1 μm / 64 = 1.6 nanometers. The driving electronics take multivalued bitmaps, i.e. bitmaps with N bit depth in each pixel. In order to preserve flexibility for the future each pixel is described by 8 bits, not the 6 bits that are necessary for 50 levels. Therefore pixel values from 0 to 255 are available and the values 0 to 50 are used for varying exposure. The codes 51 to 100 are used to generate higher deflections in the micromechanical pixels corresponding to negative complex amplitude in the wavefront, negative amplitudes that can be used so increase edge acuity and corner sharpness in the written pattern. Typically an exposed feature is printed with positive amplitude against a background of weak negative-

amplitude light, which creates a higher edge slope in the exposure of the feature.

The SLM is loaded with new pattern data 700 times per second and a single flash from an KrF laser (248 nm) is used to transfer the pattern on the SLM to the mask blank. Before the next flash the SLM needs to be rewritten and the stage advanced by approximately 50 μm so that individual flashes create a contiguous pattern on the mask blank. The stage moves at a constant speed of approximately 35 mm/s and a strip 2048 pixels wide is stitched together from the series of flashes. The maximum pattern length is 230 mm and a strip contains 230 mm * 2048 / 0.1 μm = 4.7 billion pixels needing 4.7 Gbyte of. A strip is written in 6.4 seconds and after a 1 second retrace the data for the next strip must be ready. However, writing could also be performed on the retrace stroke, making the writing process faster and more efficient.

The burst data flow is 750 Mbyte/s and the average is 650 Mbyte/s. Since the actual time it takes to process the data for a strip is not absolutely predictable, it was decided that a full strip should be buffered before a strip is written. In practice the strip buffer need to be even larger than 6.4 Gbyte to allow for transfer times and overlap between write and read operations in the memory. If the processing of data takes more time than that available the machine waits for the data before starting the strip. An abortion of the writing stroke midways due to data starvation is a more irregular and undesirable event than waiting for data in the idle position outside the plate. Therefore a system with small data buffers and a rasteriser that rasterizes on the fly must be designed with headroom and requires roughly twice the processing power of a strip-buffered system. Despite the large amounts of buffer memory needed a full strip buffering has been considered to be more cost-effective than increasing the rasterizing speed.

However, it is also possible, within the scope of the invention, not to use such large buffers, or even no buffers at all, whereby each window to be written is instead rendered and rasterized sequentially.

Parallel operation

The input data format can be in many different formats, e.g. hierarchical GDSII, flat MEBES format or in algorithmic form. The input data files can be extremely large and it is not uncommon to have pattern files that are 10 - 30 Gbyte. In the future the file size will be even higher, although there is a development towards more hierarchical files.

The SLM offers the possibility of extremely high speeds (in pixels per second) which will be needed to achieve reasonable writing times with the much smaller pixel size that is necessary for the masks of the future. In order to preserve the writing time for reticles while following More's law in terms of resolution and complexity the number of pixels per second must be doubled every 18 months. Therefore it is anticipated that any architecture where all the data must pass a single interface will sooner or later be obsolete and inadequate. Only truly parallel data processing can be scaled to arbitrary capacity. The following describes how such a truly parallel architecture can be designed:

The surface of the SLM is divided into a set of SLM fields. In the case of a an SLM with high aspect ratio (e.g. 2048 x 512 pixels) it is useful to divide it into 512 x 512 pixel fields. The data is written into the SLM by scanning. In the preferred embodiment a single DAC is scanned by an analog multiplexor over 64 column lines and charges each of them to a potential in the range 0 - 40 volts. Then a gate (row) line is opened and the charge on the column line is transferred to the storage capacitor of each pixel. Several DACs, each scanned over 64 column lines, are needed to drive the entire SLM. For an SLM

with 2048 columns there are 32 DACs. During the loading of a full image all 512 rows must be scanned and for each row all 64 columns must be scanned and charged in sequence. To load a complete image in 1 millisecond the DAC must generate 32 million voltages per second, in practice 40 M conversions per second is a more appropriate figure. This is doable with ordinary methods for design and manufacture of PC boards and electronics.

In order to increase the flexibility the SLM is designed so that it can be configured for 8, 16, 32 or 64 DACs per 2048 columns. This allows for different configurations using the same chip: with 64 DACs the SLM can be reloaded in 0.5 millisecond with the same 40 MHz conversion rate. On the other hand it is possible to build a less expensive system for a cost sensitive application with less speed requirements using 8 or 16 DACs. The basic configuration into blocks of 32 columns for one analog multiplexor makes it easy to design a larger or smaller SLM and to use the same external electronic building blocks to drive it.

In the preferred embodiment the interface between the rasterizing cabinet and the SLM are at the analog voltage after the DAC. On the PC board with the SLM there is one analog (video) input for each group of 32 together with lines for selection, timing and control, as is schematically illustrated in Fig 6. The video is in the range 0 to 1 volt and at each input on the SLM board there is an analog amplifier bringing the voltage span to the 0-40 needed for the SLM. The DACs are placed in a separate cabinet together with the rasterizing electronics. This brings true scalability, since it is possible to multiply the number of cabinets. The entire rasterizer need not fit into one backplane or one cabinet, since the high-speed interface between the rasterizer and the SLM board is the video cable which is insensitive to distance.

The DACs are combined in DAC blocks of 8 DACs corresponding to 512 columns in the SLM. Each DAC has its signal conditioning electronics including lookup tables for response curve correction. For each DAC block there is a common buffer memory and a bank of parallel rasterizing processors. Each rasterizing processor is assigned to a range of column addresses, i.e. to a band through the SLM. In the preferred embodiment a single graphics processor rasterizes the full width of the DAC block, 512 columns, but in future implementations of the architecture it is anticipated that the DAC block needs to be sub-divided between several rasterizing processors. The rasterizing processor is set up to create a bitmap in a rasterizing window, in the preferred embodiment 640 columns x 2560 rows pixels. The larger rasterizing window, or extended bitmap, than what is later going to be used (512 columns) makes it possible to correct for interaction between pattern features by operations on the bitmap. Without the extended bitmaps any interaction from features outside the 512 column field would be lost. There is a similar extension between fields in the row direction. The data in the extension is redundant and only used for computing the interactions. There is a software-controlled window that determines how much redundant data is generated outside the 512 columns.

Referring to Fig 3, a schematic multiprocessor architecture is illustrated with multiple fracturing processors and multiple rasterization processors each creates data for a contiguous area in the SLM, whereas Fig 4 schematically shows a completely parallel architecture with two completely independent units each with several fracturing processors and several rasterizing processors feeding separate areas of the SLM.

The rasterizer (R) is fed data from a FIFO buffer, data that come from a fracturing module (F) having 4 fracturing processors. In the fracturing module the input file is cut to a rasterizing field corresponding to the

extended bitmap of the rasterizing processor, and the data elements are preconditioned for the rasterizer, e.g. polygons are cut into triangles and/or trapezoids. For a hierarchical file the tree structure of the hierarchy must be partly resolved before it is cut into fracture fields. Therefore the rasterizing module must in the worst case see the entire file before it is cut up into fields. For very large files this creates a bottleneck. There are a couple of possible ways to alleviate this:

- inclusion in the hierarchical file format of size information in the header of each cell, so that cells outside of the fracture window can be skipped. Since the cell that is skipped can in itself have an internal hierarchy a lot of redundant work can be avoided.
- the CAD system that produces the file writes it with large features cut into smaller pieces, the hierarchy partly resolved and the data sorted so that the file can be read sequentially without risk of missing a feature.

With the combination of the two principles the file can be processed sequentially and redundant information is quickly discarded. It is then possible to process the entire file in each fracture module but fractured output data is only generated for those areas that are assigned to the specific fracture module. In this way four different copies of the file can be read and processed by the fracture processor, each producing fracture data for a band in the SLM and sending it to the rasterizer assigned to the same band.

In an alternative embodiment, one or several fracturing modules are connected to a plurality of rasterizing modules. Each rasterizing module preferably corresponds to a specific area of the SLM. The outputs from the rasterizing modules are fed to an SLM drive unit (SDU), which combines the rasterized data from several

rasterizing modules. From the SDU the bitmaps are transferred to the SLM through DAC:s.

In order to achieve an efficient parallel fracturing process, it is preferred to pre-treat the input data and convert it to a vector format, a so-called MIC-format. Fracturing is the process to slice a pattern in strips in Y direction. If fracturing is going to be done in real time the big input data files is preferably sorted or blocked in units, so-called buckets, in the y-direction, i.e. the direction perpendicular to the strip direction. However, this is not necessary if fracturing is done off-line. Fracturing of the data in the MIC-format, sorted in e.g. bucktes, preferably comprises the step of extracting the data into strips or substrips.

The buckets are autonomic units containing all information of the pattern objects being included in the buckets, and are preferably created on-line when reading the input data file. The bucket width may be varied between buckets, but is preferably defined at the start of the fracturing. The bucket extraction may take place in the fileserver computer or in the real time fracturing computer All iterations in the y-direction with one or two instances in a certain bucket are resolved, unpacked, in the buckets in question. All objects keep its original co-ordinates. However, unresolved iterations may cross bucket borders. There are no dependencies of objects between buckets. Further, each bucket preferably comprises random-access pointers to the big data file. However, to achieve shorter access times, the data file is preferably sorted.

In the fracturing process, one processor preferably starts to read the first bucket, if data is bucket sorted, or else from the complete file, and extracts only the first scanstrip. All other information is at this time ignored. The next processor reads the same bucket and extracts only the next scanstrip. The third processor extracts the third scanstrip and so on until all

processors are busy. This provides an efficient multi-processor fracturing. However, it is also possible to have several processors working on the same scanstrip.

Response-curve correction

The input pattern is specified as a geometry, but the response from voltage to geometry is highly non-linear. The rasterizer, which determines how much area of the pattern falls on a particular pixel and translates the area into a value between - in the preferred embodiment - 0 and 64. Since the response function is non-linear the pixel values determined by the rasterizer do not correspond to the voltages that the pixels need to be set to create an even division in sub-pixel addresses. There are different ways to make the correction, and some are discussed in PCT patent application SE99/00310. Basically the correction can be done by a non-linear analog function, such as a diode network, or by a mathematical transformation of the pixel value. An obvious correction is a polynomial up to some degree. The zeroth polynomial term is the offset, the first is the amplification factor and higher terms correct for non-linearities. The correction can be applied either when the pattern is rasterized or before it is loaded into the SLM. It is more practical to apply the correction by means of a look-up table than to actually compute the polynomial. The lookup table does in the most simple form store a single correction function that is applied to every pixel. This function represents the typical pixel non-linearity and can be empirically calibrated or derived from a physical model of the system.

For a high-end pattern generator the image uniformity is extremely important. Imperfections in the micromechanic pixel elements and differences from pixel to pixel due to ageing effects can ruin the image quality. Therefor it is highly desirable to have a pixel-by-pixel correction of the response function. Again this

can be implemented in several ways, but in the preferred embodiment a variety of the lookup table is used:

The response functions of the pixels are classified into a number of typical response curves. These are stored in a lookup memory with 24 bit input address and 16 bit output data. Each curve translates an eight-bit data value to a sixteen-bit DAC value. The architecture, which is illustrated in Fig 7, supports 16 bit DAC words, but in the preferred embodiment only the 10 most significant bits are actually used in the DAC.

There is room for 2^16 = 65536 possible curves selected by 16 bits. The 16 bits are divided into 4 bits for offset voltage, 4 bits for mirror compliance and 8 bits for brightness. Once the pixel properties, the first 2 x 4 bits, are calibrated it is easy to change the brightness of the pattern by just changing the brightness bits. In a more complex scheme, double translation, the brightness values are translated once more in a small lookup memory, the benefit being that the small lookup table can be rewritten by the machine CPU between flashes. A double translation system gives high flexibility and makes it possible to expose different areas with a dynamically changing dose, e.g. for correction in a single pass of the accumulated dose errors from a series of overlapping writing passes with displaced SLM fields between the passes. This is schematically illustrated in Fig 5.

Of course other representations can be used. Small subsets of the curves are computed, but most of them are created by linear interpolation between the computed curves. In this way the computation effort of creating 65536 curves is managable.

There is a pixel parameter memory which has one 16-bit cell for each pixel in the SLM. When a specific pixel is loaded into the SLM its 8-bit data value is translated by the lookup memory to a 16-bit word. Which curve is used is determined by the 16-bit word that is read from

the pixel parameter memory and fed to the remaining 16 address bits of the lookup memory.

Alternatively, it is also possible to use a device for arithmetic calculation of response values instead of using lookup tables. It is also possible to use any kind of hybrid solution combining arithmetic calculations and lookup memories.

Similar correction functionality is suitably used for other types of spatial energy beam modulators, such as those mentioned above.

Data integrity and error recovery

A photomask can contain 150 mm x 150 mm / (0.1 μm x 0.1 μm) pixels = 2.25 x 10^{12} pixels per writing pass. Bit errors in the data could result in point defects in the written pattern. Bit errors are often the result of electronic interference and often occur in bursts in which case the chip produced using the photomask could malfunction. In the preferred embodiment the data is transferred together with a checksum, and an error flag is raised if the checksum is wrong. This is done for all high volume data flows all the way up the DAC latch. When an error condition is raised the following laser pulse is inhibited and the writer enters a recovery mode that continues the writing from the inhibited flash when the error condition is removed. A number of other internal conditions raise the error flag, e.g. when data is not ready.

The sequence of laser pulses is also monitored so that the absence of a laser pulse within a predetermined period after the laser trig signal raises an error condition. Since the pulse is missing there was no exposure and the mask blank has not been destroyed by the error. Therefore a normal error recovery sequence including stopping the data flow, stopping the mechanical stroke (or continuing the normal stroke without exposing), backing the data, restarting the same strip

again and turning on the laser at the flash that was missing. Other error conditions that are treated in the same way are stage position errors above a predetermined limit, air pressure surges. Any condition or event that carries a risk of a writing error can be treated in the same manner with, for infrequent events, very low throughput penalty. The datapath is therefore designed with the capability of a quick reloading of the last SLM bitmap. Data transfer errors earlier in the data path cause refracture and rerasterization of some data.

CLAIMS

What is claimed is

1. A method for converting with high throughput and precision pattern data in a symbolic input format, e.g. GDSII, to a multivalued bitmap and feeding said bitmap to an analog spatial energy beam modulator (SEBM) in a pattern generator,

comprising the steps of

accepting the input format and fracturing it to fracture fields in at least one fracture processor,

sending fractured data for a fracture field to a rasterization module with at least one rasterizing processor,

rasterizing in said rasterizing processor at least part of the data to a contiguous bitmap corresponding to an area on the SEBM

and loading said contiguous bitmap into said area of the SEBM.

2. A method as described in claim 1 where during the loading of the bitmap data into the SEBM, a multivalued datum for a pixel is converted to an analog multivalued electromagnetic quantity.

3. A method as described in claim 2 where said electromagnetic quantity is an electric potential.

4. A method as described in claim 1 where the bitmap data is corrected for non-linearities in the response of the SEBM or for pixel-to-pixel variations.

5. A method as described in claim 4 where data for one pixel is corrected by lookup in a prestored lookup table.

6. A method as described in claim 5 where said table lookup is based on data value and pixel location in the SEBM.

7. A method as described in claim 5 where said table lookup is based on pixel value and one of a set of response functions for a pixel corresponding to variation

of at least one physical parameter. 8. A method as described in claim 7 where said physical parameter include at least one of the following:

- electronic offset
- electronic gain
- mechanical stiffness of a mirror
- built-in stress
- wavefront flatness
- beam pointing
- light efficiency, e.g. reflection or transmission
- a memory effect

9. A method as described in claim 4 where data for one pixel is corrected by means of arithmetic calculation.

10. A method as described in claim 1 where there are at least two rasterizing modules.

11. A method as described in claim 10 where the surface of the SEBM is divided into subfields and one rasterizing module is permanently assigned to a subfield.

12. A method as described in claim 11 where the fracture fields corresponds to the subfields of the SEBM.

13. A method according to any one of the preceding claims, wherein the spatial energy beam modulator (SEBM) is a spatial light modulator (SLM).

14. A method for converting with high throughput and precision pattern data in a symbolic input format, e.g. GDSII, to a multivalued bitmap and feeding said bitmap to an analog spatial energy beam modulator (SEBM) in a pattern generator,

comprising the steps of

accepting the input format and fracturing it to fracture fields in at least one fracture processor,

assigning a contiguous area of the SEBM to a contiguous area in the input pattern description,

sending fractured data for said pattern area to a rasterizing module having at least on rasterizing processor,

rasterizing in said rasterizing module at least part of the data to a contiguous bitmap,

and loading said bitmap into said area of the SEBM.

15. A method as described in claim 14 where at least two contiguous areas of the SEBM are assigned to two areas in the input data and sent to two rasterizing processors.

16. A method as described in claim 14 where at least two fracture processors send data to at least two rasterizing processors.

17. A method as described in claim 14 where one fracture processor sends data to at least one rasterizing processor and another fracture processor sends data to at least one rasterizing processor not receiving data from the first fracture processor.

18. A method as described in claim 17 where there is a fixed association between fracture processors and rasterizing processors.

19. A method as described in 14 where one fracture module sends data to at least one rasterizing module containing at least two rasterizing processors.

20. A method as described in 14 where one fracture module containing at lest two fracture processors send data to at least one rasterizing module containing at least two rasterizing processors.

21. A method as described in 14 where one fracture module sends data to one rasterizing module and another fracture module sends data to a different rasterizing module.

22. A method according to any one of the claims 14-21, wherein the spatial energy beam modulator (SEBM) is an spatial light modulator (SLM).

23. A method for converting with high throughput and precision pattern data in a symbolic input format,

e.g. GDSII, to a multivalued bitmap and feeding said bitmap to an analog spatial energy beam modulator (SLM) in a pattern generator,

comprising the steps of

accepting the input format and fracturing it to fracture fields in at least one fracture processor,

tagging the data in the fracture fields with their intended position in the pattern,

sending fractured and tagged fields to at least one rasterizing module,

rasterizing in said rasterizing module at least part of the tagged fracture data to tagged bitmaps,

and loading said bitmaps into areas of the SEBM determined by the tags.

24. A rasterizer for converting with high throughput and precision pattern data in a symbolic input format, e.g. GDSII, to a multivalued bitmap and feeding said bitmap to an analog spatial energy beam modulator (SEBM) in a pattern generator, comprising

an input channel, e.g. a network connection or a station for mountable media, for input pattern data,

a fracture module for fracturing said input data into fracture fields

a rasterization module for rasterizing data for the fracture fields into multivalued bitmaps,

a transfer structure, e.g. a bus or a serial data interface, for loading said bitmaps into said SEBM.

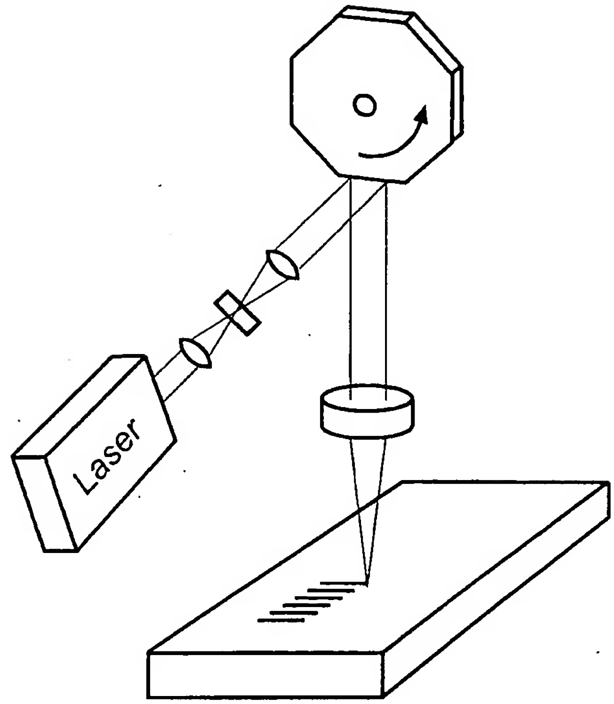
Laser

Fig. 1a

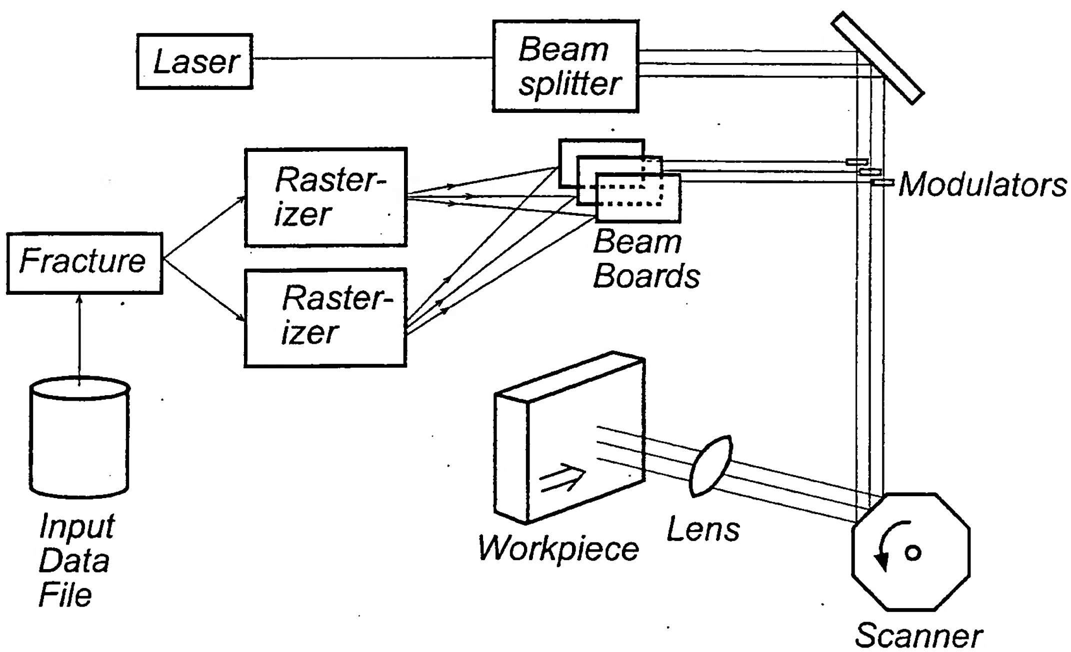
Laser
Beam splitter
Raster-izer
Raster-izer
Modulators
Beam Boards
Fracture
Input Data File
Workpiece
Lens
Scanner

Fig. 1b

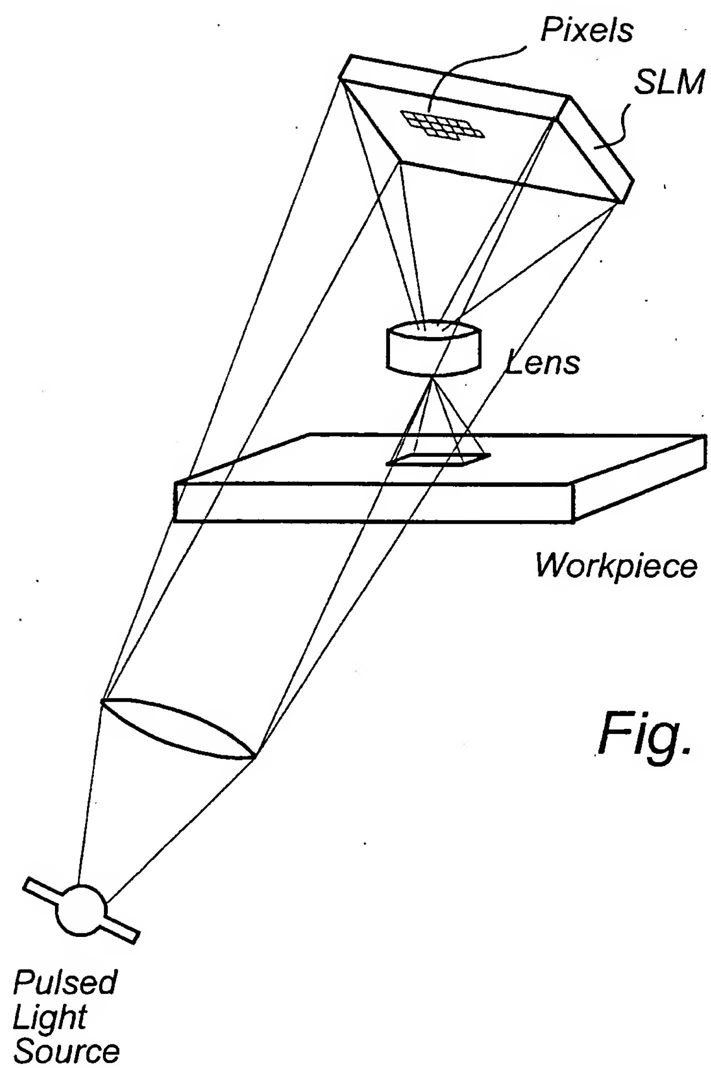

Fig. 2

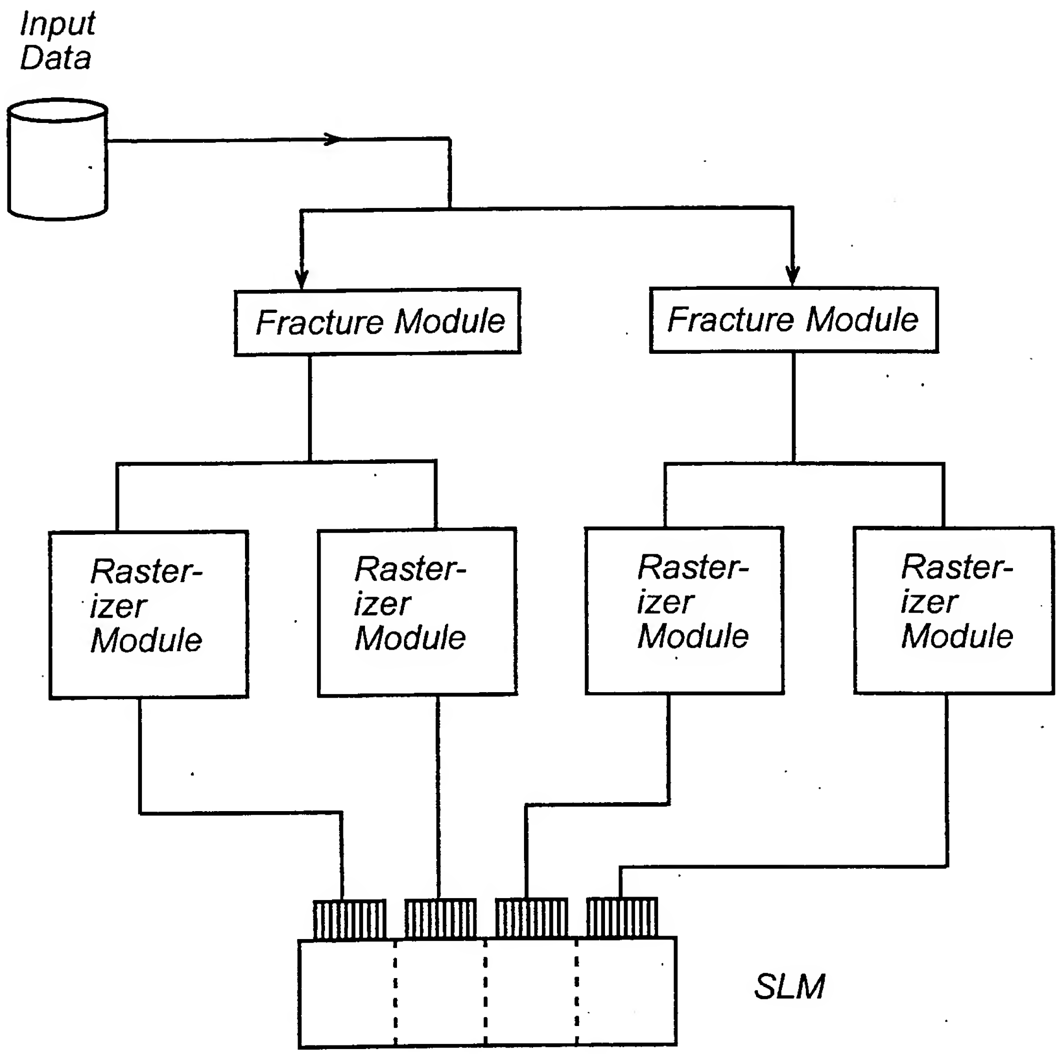
Input Data
Fracture Module
Fracture Module
Raster-izer Module
Raster-izer Module
Raster-izer Module
Raster-izer Module
SLM

Fig. 3

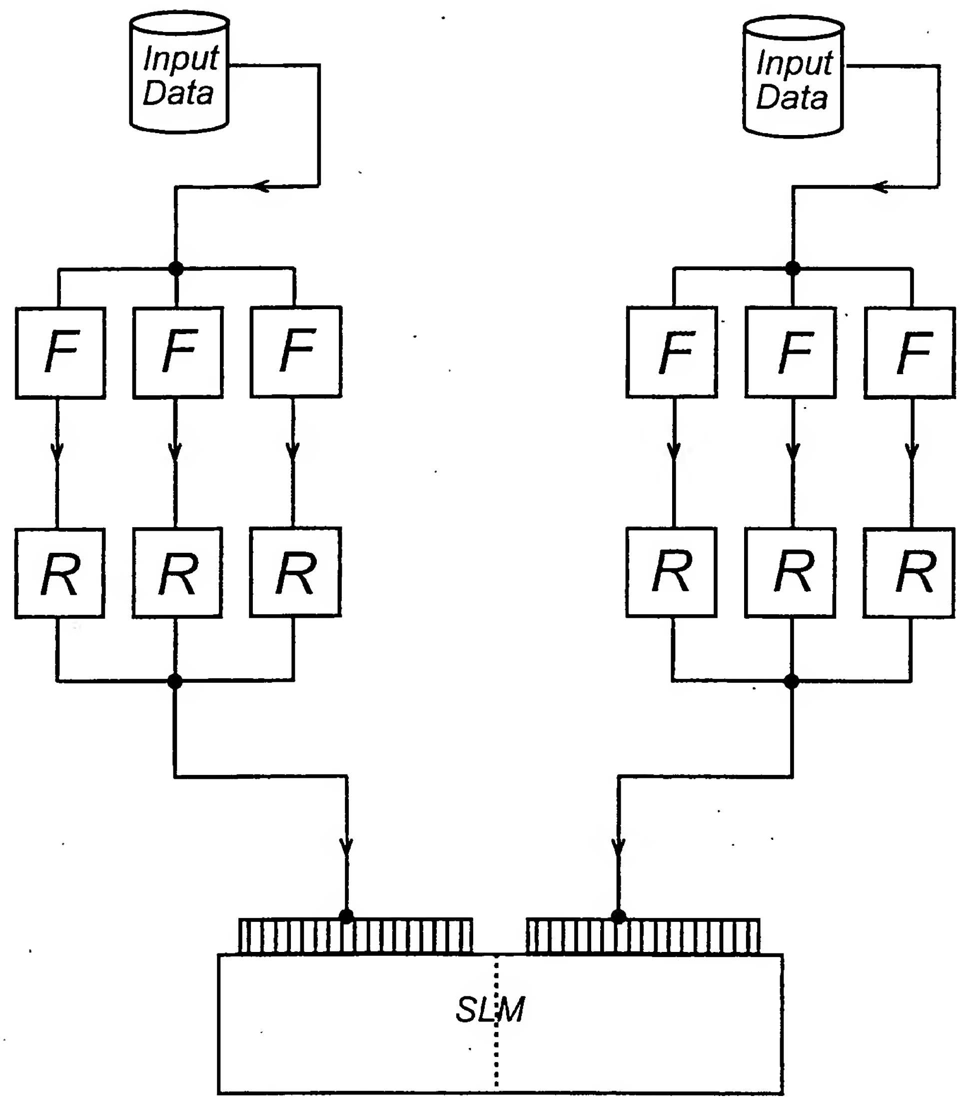

Fig. 4

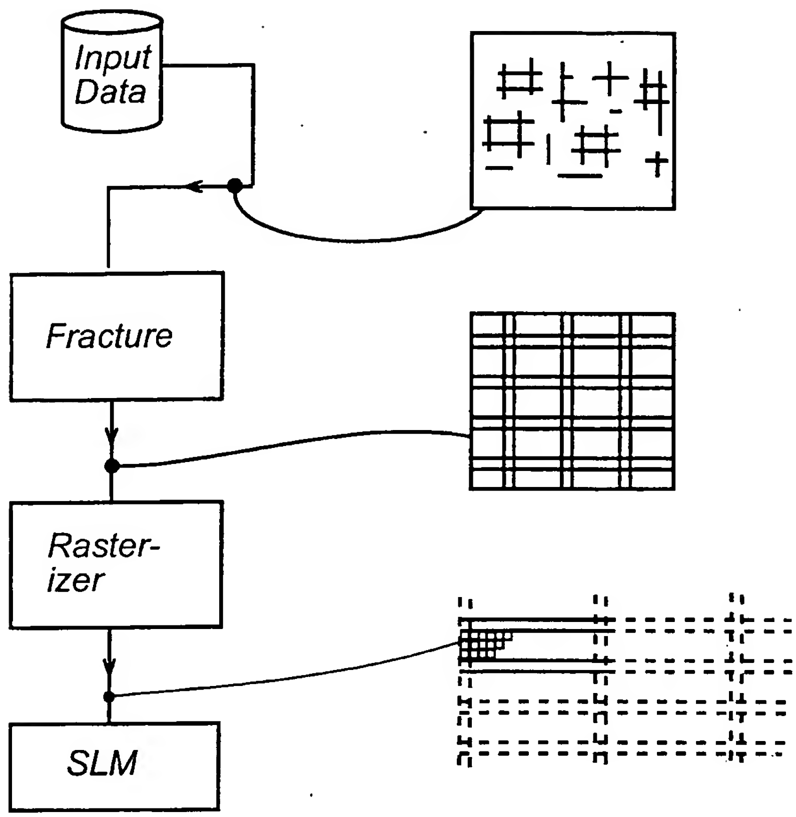

Fig. 5

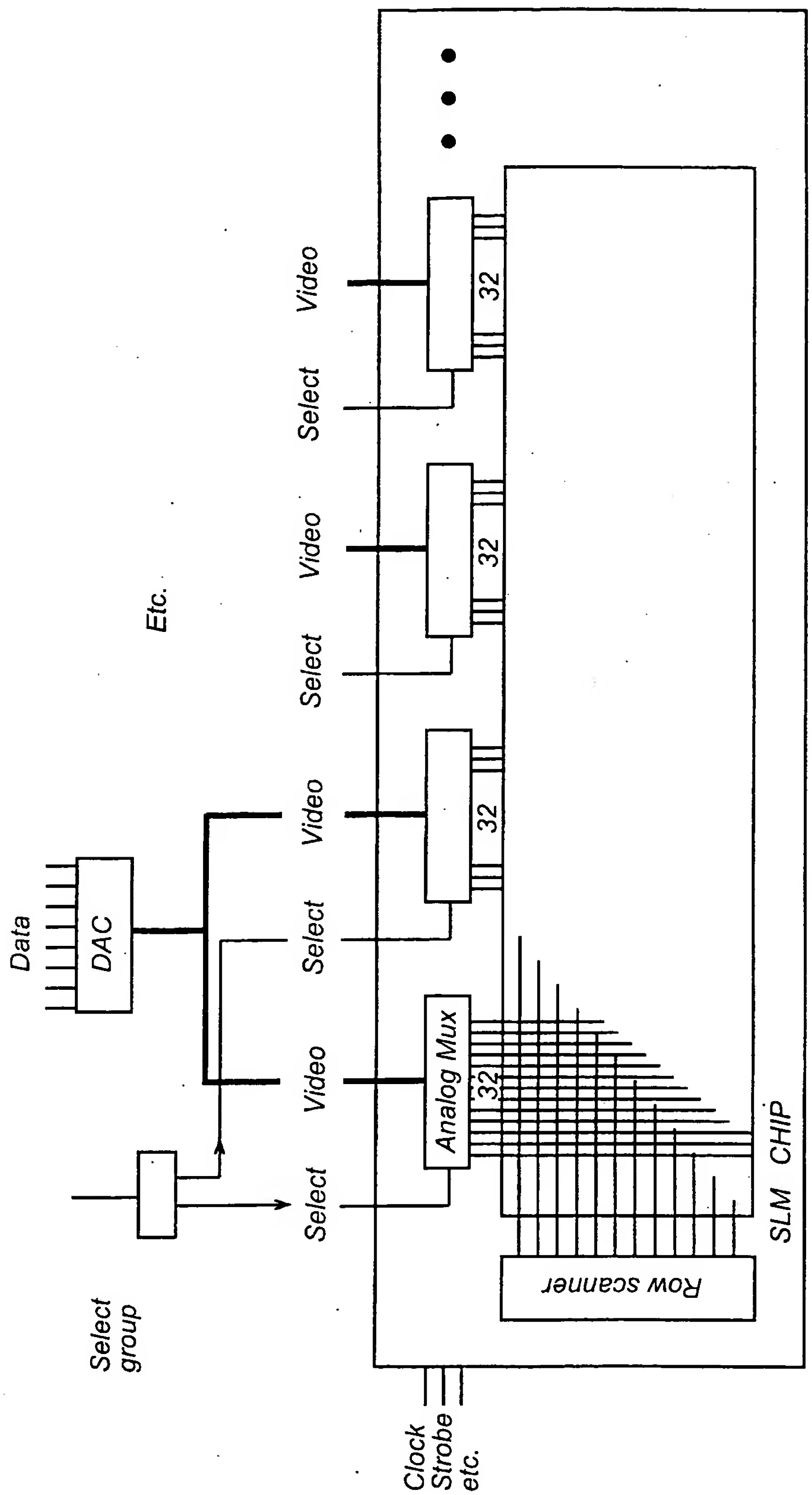
Data
DAC
Select group
Select
Video
Select
Video
Select
Video
Select
Video
Etc.
Analog Mux
32
32
32
32
Row scanner
SLM CHIP
Clock
Strobe
etc.

Fig. 6

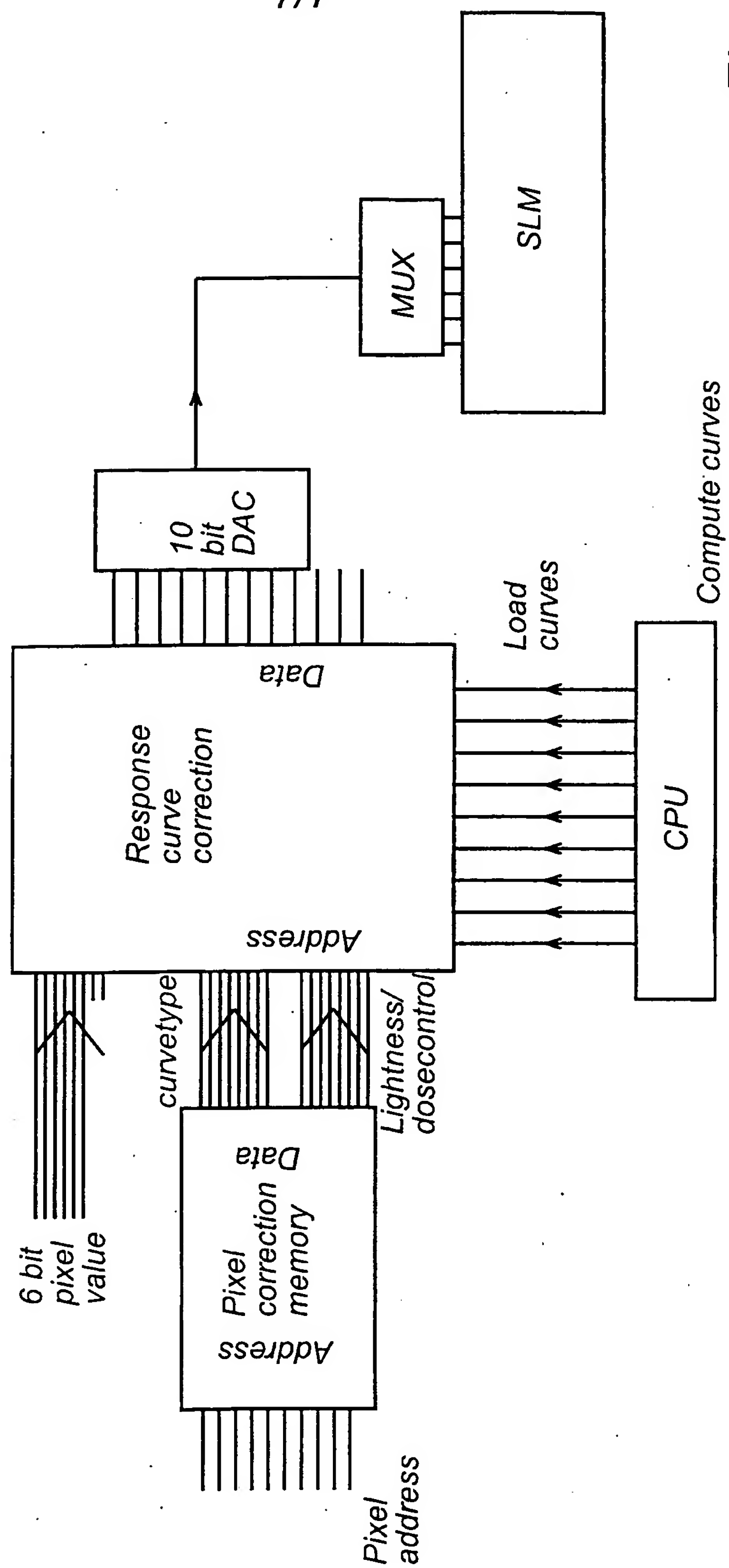
SLM
MUX
10 bit DAC
Data
Response curve correction
Address
Load curves
Compute curves
CPU
curvetype
Lightness/ dosecontrol
6 bit pixel value
Data
Pixel correction memory
Address
Pixel address

Fig. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 00/01749

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: G03F 7/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

QUESTEL: EDOC, WPIL, JAPIO, DIALOG: DIALINDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5631721 A (STUART STANTON ET AL), 20 May 1997 (20.05.97), column 3, line 54 - line 61, figure 1 --	1-24
A	US 5864146 A (ANDREW KARELLAS), 26 January 1999 (26.01.99), column 32, line 44 - line 67; column 33, line 52 - line 53 -- --------	1-24

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 December 2000	13 -12- 2000
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Bengt Christensson/MP Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

Information on patent family members

04/12/00

International application No.
PCT/SE 00/01749

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5631721 A	20/05/97	CA 2177196 A	25/11/96
		EP 0744664 A	27/11/96
		JP 9007940 A	10/01/97
US 5864146 A	26/01/99	CA 2254877 A	20/11/97
		EP 0914060 A	12/05/99
		WO 9742877 A	20/11/97